UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,076	01/20/2004	Chun-ying Chen	1875.5720000/RES/GSB	7164

26111 7590 04/21/2005

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,076	CHEN ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,7 and 9* is/are rejected.

7)☒ Claim(s) *3,5,8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 402A, 402B and 404 in fig. 4B. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Claims 1-10 are objected to because of the following informalities: Claims 1, 2, 4, 5, 6, 7, 9 and 10, the word "MOS" should be in full written form. Claims 1, 2, 4, 5, the word "NWELL" should be in full written form. Claims 2, 3, 4, 5, the word "PMOS" should be in full written form. Claims 6, 7, 9, 10, the word "PWELL" should be in full written form. Claims 7, 8, 9, 10, the word "NMOS" should be in full written form. Appropriate correction is required.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The first and second NMOS transistors and the first and

second MOS-on-PWELL devices in claim 7. The first and second MOS-on-PWELL devices and the first and second NMOS transistors in claim 9. All the claimed subject matters as claimed in each of claims 5, 6, 8 and 10.

4. Claims 2, 4, 7 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 10-11, claim 4, lines 8-9, the phrase "a combination of the first and second PMOS transistors are connected in parallel with the first and second MOS-on-NWELL devices" is vague and indefinite. Fig. 5A discloses the first gate, the second pickup terminal, the gate of the first PMOS and the source and drain terminals of the second PMOS are connected to a first common terminal. In addition, the second gate, the first pickup terminal, the gate of the second PMOS and the source and drain terminals of the first PMOS are connected to a second common terminal. Claim 2 can be rewrite as describe in the preceding sentence.

Claim 7, lines 10-11, the phrase "a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices" is vague and indefinite. Since claim 1 never discloses first and second MOS-on-PWELL devices, it is unclear how the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices. Are the first and second MOS-on-PWELL devices also included in the capacitor structure?

Claim 9, lines 8-9, the phrase "a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices"

is vague and indefinite. Since claim 3 never discloses first and second NMOS transistors, it is unclear how the first and second MOS-on-PWELL devices are connected in parallel with the first and second NMOS transistors. Are the first and second NMOS transistors also included in the capacitor structure?

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Horiguchi et al.

In regards to claim 1, Horiguchi et al. show all the elements of the claimed invention in fig. 34C. It is a capacitor for an integrated circuit, comprising: a first MOS-on-NWELL device (the MOSFET and the N-WELL on the left of the figure) formed on a substrate [101] and having a first pickup terminal (the terminal that connected to the n-type region [103]) and a first gate [106]; a second MOS-on-NWELL device (the MOSFET and the N-WELL on the right of the figure) formed on the substrate [101] and having a second pickup terminal (the terminal that connected to the n-type region [103]) and a second gate [106], wherein the first gate is connected to the second pickup terminal, and wherein the second gate is connected to the first pickup terminal.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al.

In regards to claim 6, Horiguchi et al. differ from the claimed invention by not showing a capacitor for an integrated circuit comprising: a first MOS-on-PWELL device formed on a substrate and having a first pickup terminal and a first gate; a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate, wherein the first gate is connected to the second pickup terminal, and wherein the second gate is connected to the first pickup terminal.

It would have been obvious for the capacitor for an integrated circuit comprising: a first MOS-on-PWELL device formed on a substrate and having a first pickup terminal and a first gate; a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate, wherein the first gate is connected to the second pickup terminal, and wherein the second gate is connected to the first pickup terminal because it is conventional to reverse the conductivity type of all the regions of Horiguchi et al. device to form a device complement to that of Horiguchi et al.

9. Claims 3, 5, 8 and 10 would be allowable if rewritten or amended to overcome the objections set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor, and a gate of the second PMOS transistor is connected to the

source and drain terminals of the first PMOS transistor. The second major difference in the claims not found in the prior art of record is a first plurality of PMOS transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors, and a second plurality of PMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors. The third major difference in the claims not found in the prior art of record is a gate of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor, and a gate of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor. The fourth major difference in the claims not found in the prior art of record is a first plurality of NMOS transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors, and a second plurality of NMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
April 17, 2005

Steven Loke